# EXCEL ENGINEERING COLLEGE
## (Autonomous)

**Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai**
**Accredited by NBA and NAAC with "A+"and Recognized by UGC(2f&12B)**
**KOMARAPALAYAM – 637303**

**DEPARTMENT OF EEE REGULATION 2022**

**M.E – EMBEDDED SYSTEM TECHNOLOGIES**

**Curriculum for Semesters – I to IV**

| **I – SEMESTER** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **Periods / Week** | | | **C** | **Maximum Marks** | | |
| | | | **L** | **T** | **P** | | **CA** | **FE** | **Total** |
| **Theory Course(s)** | | | | | | | | | |
| 22PMA104 | Applied Mathematics for Electronics Engineers | FC | 3 | 2 | 0 | 4 | 40 | 60 | 100 |
| 22PES101 | VLSI Design and Reconfigurable Architecture | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PES102 | Microcontroller Based System Design | PC | 3 | 2 | 0 | 4 | 40 | 60 | 100 |
| 22PES103 | Design of Embedded Systems | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESEXX | Professional Elective I | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESEXX | Professional Elective II | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| **Practical Course** | | | | | | | | | |
| 22PES104 | Embedded System Laboratory-I | PC | 0 | 0 | 4 | 2 | 50 | 50 | 100 |
| | | **Total** | **18** | **4** | **4** | **22** | **290** | **410** | **700** |

| **II- SEMESTER** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **Periods / Week** | | | **C** | **Maximum Marks** | | |
| | | | **L** | **T** | **P** | | **CA** | **FE** | **Total** |
| **Theory Course(s)** | | | | | | | | | |
| 22PES201 | Real Time Operating Systems | PC | 3 | 2 | 0 | 4 | 40 | 60 | 100 |
| 22PES202 | Python Programming With Machine Learning | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PES203 | RISC Processor Architecture and Programming | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PES204 | Internet of Things | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESEXX | Professional Elective-III | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESEXX | Professional Elective-IV | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

Passed in Board of Studies Meeting (24.02.2022) Approved in Academic Council Meeting (09.03.2022)

**Chairman – Board of Studies**

| **Practical Course** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 22PES205 | Embedded System Laboratory-II | PC | 0 | 0 | 4 | 2 | 50 | 50 | 100 |
| | | **Total** | **18** | **2** | **4** | **21** | **290** | **410** | **700** |

**III – SEMESTER**

| **Code No.** | **Course** | **Category** | **Periods / Week** | | | **C** | **Maximum Marks** | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | **L** | **T** | **P** | | **CA** | **FE** | **Total** |
| **Theory Course(s)** | | | | | | | | | |
| 22PTE301 | Research Methodology and IPR | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PES302 | Wireless And Mobile Communication | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESEXX | Professional Elective V | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| **Practical Course** | | | | | | | | | |
| 22PES303 | Project Work Phase- I | EEC | 0 | 0 | 12 | 6 | 50 | 50 | 100 |
| | | **Total** | **9** | **0** | **12** | **15** | **170** | **230** | **400** |

**IV- SEMESTER**

| **Code No.** | **Course** | **Category** | **Periods / Week** | | | **C** | **Maximum Marks** | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | **L** | **T** | **P** | | **CA** | **FE** | **Total** |
| **Practical Course** | | | | | | | | | |
| 22PES401 | Project Work Phase -II | EEC | 0 | 0 | 24 | 12 | 50 | 50 | 100 |
| | | **Total** | **0** | **0** | **24** | **12** | **50** | **50** | **100** |

**LIST OF PROFESSIONAL ELECTIVES**

| **Code No.** | **Course** | **Category** | **Periods / Week** | | | **C** | **Maximum Marks** | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | **L** | **T** | **P** | | **CA** | **FE** | **Total** |
| **Theory Course(s)** | | | | | | | | | |
| **Semester I- Elective I** | | | | | | | | | |
| 22PESE01 | ASIC and FPGA Design | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE02 | Advanced Computer Architecture and Parallel Processing | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE03 | Digital Instrumentation | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| | | | | | | | | | |
| **Semester I- Elective II** | | | | | | | | | |
| 22PESE11 | Device Driver Embedded Linux | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE12 | Advanced Digital Signal Processors | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 22PESE13 | Embedded & Real Time Systems | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| **Semester II- Elective III** | | | | | | | | | |
| 22PESE21 | Embedded Product Development | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE22 | Electric Vehicles and Power Management | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE23 | Reconfigurable Processor and SoC Design | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| **Semester III- Elective IV** | | | | | | | | | |
| 22PESE31 | Digital Image Processing | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE32 | Embedded Networking and Automation of Electrical System | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE33 | Smart System Design | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Semester III- Elective V** | | | | | | | | | |
| 22PPEE43 | Smart Grid | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE42 | Soft Computing and Optimization Techniques | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE43 | Cryptography And Network Security | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE44 | Robotics and Control | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 22PESE45 | Digital Signal Processors | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

| S. No | Category | CREDITS PER SEMESTER | | | | Total Credit (AICTE) | Credits in % |
|---|---|---|---|---|---|---|---|
| | | I | II | III | IV | | |
| 1 | FC | 4 | | | | 4 | 5.71% |
| 2 | BS | | | | | | |
| 3 | ES | | | | | | |
| 4 | PC | 12 | 15 | 6 | | 33 | 47.14% |
| 5 | PE | 6 | 6 | 3 | | 15 | 21.42% |
| 6 | OE | | | | | | |
| 7 | EEC | | | 6 | 12 | 18 | 25.71% |
| Total | | 22 | 21 | 15 | 12 | 70 | 100.00% |

FC – Foundation Courses

BS - Basic Sciences

ES - Engineering Sciences

PC - Professional Core

PE - Professional Electives

OE - Open Electives

EEC - Employability Enhancement Courses

CA - Continuous Assessment

FE - Final Examination

**I SEMESTER**

| 22PMA104 | APPLIED MATHEMATICS FOR ELECTRICAL ENGINEERS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 2 | 0 | 4 |
| **Nature of Course** | Fundamental Core | | | | |
| **Pre requisites** | Basic Engineering Mathematics | | | | |

**Course Objectives**
**The course is intended to**

1. The main objective of this course is to demonstrate various analytical skills in applied mathematics.
2. Understand the extensive experience with the tactics of problem solving and logical thinking applicable for the students of electrical engineering.
3. To study performance of mathematical tools from a variety of mathematical areas, including matrix theory.
4. To study identify, formulate, abstract, and solve problems in electrical engineering.
5. To study the calculus of variations, probability, linear programming and Fourier series.

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| CO1 | Apply various methods in matrix theory to solve system of linear equations | Apply |
| CO2 | Maximizing and minimizing the functional that occur in electrical engineering discipline | Analyze |
| CO3 | Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable | Apply |
| CO4 | Could develop a fundamental understanding of linear programming models, able to develop a linear programming model from problem description, apply the simplex method for solving linear programming problems | Apply |
| CO5 | Fourier series analysis and its uses in representing the power signals | Analyze |

**Course Contents:**

**UNIT I MATRIXTHEORY 12**

Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

**UNIT II CALCULUS OF VARIATIONS 12**

Concept of variation and its properties – Euler's equation – Functional dependant on first and higher order derivatives – Functionals dependant on functions of several independent variables – variation problems with moving boundaries – Isoperimetric problems - Direct methods : Ritz and Kantorovich methods.

**UNIT III PROBABILITY ANDRANDOMVARIABLES 12**

Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Randomvariable.

**UNIT IV LINEAR PROGRAMMING 12**

Formulation – Graphical solution – Simplex method – Big M method - Two phase method - Transportation and Assignment models.

**UNIT V FOURIER SERIES 12**

Fourier trigonometric series: Periodic function as power signals – Convergence of series – Even and odd function : Cosine and sine series – Non periodic function : Extension to other intervals - Power signals : Exponential Fourier series – Parseval's theorem and power spectrum – Eigen value problems and orthogonal functions – Regular Sturm - Liouville systems – Generalized Fourier series.

**TOTAL: 60 PERIODS**

**REFERENCES:**


1. Andrews L.C. and Phillips R.L., "Mathematical Techniques for Engineers and Scientists", Prentice Hall of India Pvt. Ltd., New Delhi, 2019.
2. Bronson, R. "Matrix Operation", Schaum's outline series, 2nd Edition, McGraw Hill, 2015.
3. Elsgolc, L. D. "Calculus of Variations", Dover Publications, New York, 2007.
4. Johnson, R.A., Miller, I and Freund J., "Miller and Freund's Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.
5. O'Neil, P.V., "Advanced Engineering Mathematics", Thomson Asia Pvt. Ltd., Singapore, 2003.
6. Taha, H.A., "Operations Research, An Introduction", 9th Edition, Pearson education, New Delhi, 2016.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand / Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

Passed in Board of Studies Meeting (24.02.2022) Approved in Academic Council Meeting (09.03.2022)

Chairman – Board of Studies

| 22PES101 | VLSI DESIGN AND RECONFIGURABLE ARCHITECTURE | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Core | | | | |
| **Pre requisites** | Fundamental of Embedded System | | | | |

**Course Objectives**

**The course is intended to**

1. To expose the students to the fundamentals of sequential system design, synchronous and Asynchronous circuits.
2. To understand the basic concepts of CMOS and to introduce the IC fabrication methods.
3. To introduce the Reconfigurable Processor technologies, To provide an insight and architecture significance of SOC.
4. To introduce the basics of analog VLSI design and its importance.
5. To learn about the programming of Programmable device using Hardware description Language.

**Course Outcomes**

On successful completion of the course, students will be able to

| CO No | Course Outcome | Bloom's Level |
|---|---|---|
| CO1 | Incorporating synchronous and asynchronous switching logics, with clocked circuits design. | Analyze |
| CO2 | The learning process delivers insight into developing CMOS design techniques and IC fabrication methods. | Analyze |
| CO3 | Understand the need of reconfigurable computing, hardware-software co design and operation of SoC processor. | Apply |
| CO4 | Design and development of reprogrammable analog devices and its usage for Embedded applications. | Analyze |
| CO5 | Understating and usage of HDL computational processes with improved design strategies. | Apply |

**Course Contents:**

**UNIT I INTRODUCTION TO ADVANCED DIGITAL SYSTEM DESIGN 9**

Modeling of Clocked Synchronous Sequential Network (CSSN), Design of CSSN, Design of Asynchronous Sequential Circuits (ASC), Designing Vending Machine Controller, Races in ASC, Static and Dynamic Hazards, Essential Hazards, Designing Hazard free circuits.

**UNIT II CMOS BASICS & IC FABRICATION 9**

Moore's Law-MOSFET Scaling - MOS Transistor Model-Determination of pull up / pull down ratiosCMOS based combinational logic & sequential design- Dynamic CMOS -Transmission GatesBic MOS- Low power VLSI – CMOS IC Fabrications - Stick Diagrams, Design Rules and Layout.

**UNIT III ASIC AND RECONFIGURABLE PROCESSOR AND SoC DESIGN 9**

Introduction to ASIC, ASIC design flow- programmable ASICs- Introduction to reconfigurable processor- Architecture -Reconfigurable Computing, SoC Overview, recent trends in Reconfigurable Processor & SoC, Reconfigurable processor-based DC motor control.

**UNIT IV ANALOG VLSI DESIGN 9**

Introduction to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp -High Speed and High frequency op-amps-Super MOS- Analog primitive cells- Introduction to FPAA.

**UNIT V HDL PROGRAMMING 9**

Overview of digital design with VHDL, structural, data flow and behavioural modeling concepts- logic synthesis-simulation-Design examples, Ripple carry Adders, Carry Look ahead adders, Multiplier, ALU, Shift Registers, Test Bench.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
2. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.
3. Nurmi, Jari (Ed.) "Processor Design System-On-Chip Computing for ASICs and FPGAs" Springer, 2007.
4. Joao Cardoso, Michael Hübner, "Reconfigurable Computing: From FPGAs to Hardware/Software Codesign" Springer, 2011.
5. Pierre-Emmanuel Gaillardon, Reconfigurable Logic: Architecture, Tools, and Applications, 1 st Edition, CRC Press , 2015.
6. Mohamed Ismail ,Terri Fiez, “Analog VLSI Signal and information Processing”, McGraw Hill International Editions,1994.
7. William J. Dally / Curtis Harting / Tor M. Aamodt,” Digital Design Using VHDL:A Systems Approach, Cambridge Univerity Press,2015.
8. ZainalatsedinNavabi, ‘VHDL Analysis and Modelling of Digital Systems’, 2n Edition, Tata McGraw Hill, 1998.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 3 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 3 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

**Formative assessment**

| Bloom’s Level | Assessment Component | Marks | Total marks |
|---|---|---|---|
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

**Summative Assessment**

| Bloom’s Category | Continuous Assessment Tests | | | Terminal Examination (60) |
|---|---|---|---|---|
| | IAE 1 (7.5) | IAE 2 (7.5) | IAE 3 (10) | |
| Remember | | | | |
| Understand | | | | |
| Apply | 20 | 20 | 20 | 40 |
| Analyze | 30 | 30 | 30 | 60 |
| Evaluate | | | | |
| Create | | | | |

Passed in Board of Studies Meeting (24.02.2022) Approved in Academic Council Meeting (09.03.2022)

Chairman – Board of Studies

| 22PES102 | MICROCONTROLLER BASED SYSTEM DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 2 | 0 | 4 |
| **Nature of Course** | Professional Core | | | | |
| **Pre requisites** | Basic Concepts of Microcontroller | | | | |

**Course Objectives**

**The course is intended to**

1. To introduce the fundamentals of microcontroller based system design.
2. To teach I/O and RTOS role on microcontroller.
3. To know Microcontroller based system design, applications.
4. To teach I/O interface in system Design
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| CO1 | Review of PIC controllers, learn assembly and C-programming of PIC | Understand |
| CO2 | learn Interfacing of Microcontroller | Apply |
| CO3 | Learners will study about PIC microcontroller and system design | Analyze |
| CO4 | The course would enable students to enrich their knowledge with hands on experiments and project based learning | Apply |
| CO5 | Effectively utilize microcontroller software development tools such as a compiler, make files, or compile scripts | Analyze |

**Course Contents:**

**UNITI PIC 16F627 ARCHITECTURE 9**

Introduction to PIC Microcontroller-PIC 16C6x and PIC16C7x Architecture-PIC16cxx-- Pipelining - Program Memory considerations - Register File Structure - Instruction Set - Addressing modes - Simple Operations.

**UNITII PIC 18F452 ARCHITECTURE 9**

Architecture - pin diagram - memory organization - addressing modes - instruction set - Timers - Interrupts - I/O ports, Interfacing I/O Devices – Serial Communication.

**UNITIII PERIPHERAL OF PICMICROCONTROLLER 9**

Timers – Interrupts, I/O ports- I2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing -Flash and EEPROM memories.

**UNITIV PIC 18F452 PROGRAMMING 9**

Assembly language programming – Arithmetic Instructions – Logical Instructions -Single bit Instructions – Timer Counter Programming -Integrated Development Environment (IDE) in assembling, Debugging and Executing a program using MPLAB IDE in assembly and Embedded C

**UNITV SYSTEM DESIGN –CASE STUDY 9**

Interfacing LCD Display - Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control - Controlling DC/ AC appliances - Measurement of frequency - Stand-alone Data Acquisition System.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Peatman,J.B., ¯Design with PIC Micro Controllers‖PearsonEducation,5th Edition, 2018

2. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey ' PIC Microcontroller and EmbeddedSystems using Assembly and C for PIC18', Pearson Education, 2018

3. Rajkamal,"Microcontrollers Architecture, Programming Interfacing,& System Design, Pearson, 2018.
4. Ramesh Gaonkar, Fundamentals of Microcontrollers and application in Embedded Systems (with PIC 18F Microcontroller family) penram International Publishing, first edition, 2010

**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 3 | | | | | | | | | | | | |
| CO3 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 2 | 3 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

**Formative assessment**

| Bloom's Level | Assessment Component | Marks | Total marks |
|---|---|---|---|
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

**Summative Assessment**

| Bloom's Category | Continuous Assessment Tests | | | Terminal Examination (60) |
|---|---|---|---|---|
| | IAE 1 (7.5) | IAE 2 (7.5) | IAE 3 (10) | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PES103 | DESIGN OF EMBEDDED SYSTEMS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Core | | | | |
| **Pre requisites** | Fundamental of Embedded Systems | | | | |

**Course Objectives**

**The course is intended to**

1. Toprovideaclearunderstandingonthebasicconcepts,BuildingBlocksof Embedded System.
2. To teach the fundamentals of Embedded processor Modeling , Bus Communication in processors, Input/output interfacing
3. To introduce on processor scheduling algorithms , Basics of Real time operatingsystem.
4. To discuss on aspects required in developing a new embedded processor, different Phases & Modeling of embeddedsystem
5. To involve Discussions/ Practice/Exercise onto revising & familiarizingthe concepts acquired over the 5 Units of the subject for improved employability skills

**Course Outcomes**

On successful completion of the course, students will be ableto

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| CO1 | An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical. | Analyze |
| CO2 | understand the fundamental concepts of real-time operatingsystems | Apply |
| CO3 | Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems | Analyze |
| CO4 | Design real time embedded systems using the concepts ofRTOS | Apply |
| CO5 | Foster ability to understand the role of embedded systems inindustry | Apply |

**Course Contents:**

**UNITI INTRODUCTION TOEMBEDDED SYSTEMS 9**

Introduction to Embedded Systems -Structural units in Embedded processor, selection of processor & memory devices- DMA, Memory management methods- memory mapping, cache replacement concept, Timer and Counting devices, Watchdog Timer, Real Time Clock.

**UNITII EMBEDDED NETWORKING AND INTERRUPTSSERVICEMECHANISM 9**

Embedded Networking: Introduction, I/O Device Ports & Buses- Serial Bus communication protocols - RS232 standard – RS485 -USB – Inter Integrated Circuits (I2C) – interrupt sources , Programmed-I/O busy-wait approach without interrupt service mechanism- ISR concept-– multiple interrupts – context and periods for context switching, interrupt latency and deadline -Introduction to Basic Concept Device Drivers.

**UNITIII RTOS BASED EMBEDDEDSYSTEMDESIGN 9**

Introduction to basic concepts of RTOS- Task, process & threads, interrupt routines in RTOS, Multiprocessing and Multitasking, Preemptive and non-preemptive scheduling, Task communication- shared memory, message passing-, Interprocess Communication – synchronization between processes-semaphores, Mailbox, pipes, priority inversion, priority inheritance-comparison of commercial RTOS features - RTOS Lite, Full RTOS, VxWorks, µC/OS-II, RT Linux.

**UNITIV SOFTWAREDEVELOPMENTTOOLS 9**

Software Development environment-IDE, assembler, compiler, linker, simulator, debugger, In circuit emulator, Target Hardware Debugging, need for Hardware-Software Partitioning and Co-Design. Overview of UML, Scope of UML modeling, Conceptual model of UML, Architectural, UML

basic elements-Diagram- Modeling techniques - structural, Behavioral, Activity Diagrams.

**UNIT V EMBEDDED SYSTEMAPPLICATION DEVELOPMENT 9**

Objectives, different Phases & Modeling of the Embedded product Development Life Cycle (EDLC), Case studies on Smart card- Adaptive Cruise control in a Car -Mobile Phone software for key inputs.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Rajkamal, 'Embedded system-Architecture, Programming, Design',TMH,2019.
2. Peckol, "Embedded systemDesign",JohnWiley&Sons,2010
3. Shibu.K.V, "Introduction to Embedded Systems", Tata McGrawHill,2018
4. Lyla B Das," Embedded Systems-An IntegratedApproach",Pearson2013
5. Elicia White,"Making Embedded Systems",O'ReillySeries,SPD,2011
6. Bruce Powel Douglass,"Real-Time UML Workshop for EmbeddedSystems,Elsevier,2011
7. Simon Monk, "Make: Action, Movement, Light and Sound with Arduino and Raspberry Pi", O'Reilly Series,SPD,2016.
8. Tammy Noergaard, "Embedded System Architecture, A comprehensive Guide for Engineers and Programmers", Elsevier,2006
9. JonathanW.Valvano,"Embedded Microcomputer Systems ,Real Time Interfacing",Cengage Learning,3rd edition,2012


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO2 | 3 | 3 | | | | | | | | | | 2 | | | |
| CO3 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO4 | 3 | 2 | | | | | | | | | | 1 | | | |
| CO5 | 3 | 1 | | | | | | | | | | 2 | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| Bloom's Level | Assessment Component | Marks | Total marks |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| Bloom's Category | Continuous Assessment Tests | | | Terminal Examination (60) |
| | IAE 1 (7.5) | IAE 2 (7.5) | IAE 3 (10) | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PES104 | EMBEDDED SYSTEM LABORATORY-I | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |
| **Nature of Course** | Devices and Circuits | | | | |
| **Pre requisites** | Fundamentals of Embedded Systems | | | | |

**Course Objectives**

**The course is intended to**

1. To study various controllers and different Languages/plotform.
2. To Learn Programming for microcontroller with AVR/PIC.
3. To Learn Programming with Arduino Microcontroller Board.
4. To learn Verilog HDL Programming in FPGA processors
5. To understand the concept of built in Simulation Tools as Proteus/ ORCAD/MATLAB.

**Course Outcomes**

1. The students will learn design with simulators/ programmingEnvironments
2. The students will learn design with simulators/experiments,in programming
3. Processor boards,processor interfacing/ designing digitalcontrollers
4. The students will learn design with simulators/experiments,in programming processor boards,processor interfacing/ designing digital controllers.
5. The students will learn design, modeling&simulation ofCombinational, Sequential, Synchronous, Asynchronous circuits with simulators/experimentsin programming processor boards, processor interfacing/designingreprogrammable system.

| S.No. | Course Content | CO | Bloom's Level |
|---|---|---|---|
| 1 | Programming in Higher Level Languages/ Platforms | CO1 | Apply |
| 2 | Programming with 8-bit Microcontrollers:Assembly programming Study on in circuit Emulators, cross compilers, debuggers | CO1 | Analyze |
| 3 | I/O Programming with 8-bit Microcontrollers I/O Interfacing: Timers/ Interrupts/ Serial portprogramming/PW M Generation/ Motor Control/ADC/DAC/ LCD/ RTCInterfacing/ Sensor Interfacing | CO4 | Apply |
| 4 | Programming with AVR/ PIC Microcontrollers:<br>✓ Assembly<br>✓ C programming<br>✓ programming<br>✓ Interfacing peripherals<br>Study on in circuit Emulators, cross compilers, debuggers. | CO2 | Analyze |
| 5 | I/O Programming with AVR/ PIC Microcontrollers I/O Interfacing: Timers/ Interrupts/ Serial port programming/PW M Generation/ Motor Control/ADC/DAC / LCD/ RTCInterfacing/ SensorInterfacing | CO4 | Apply |
| 6 | Programming with Arduino Microcontroller Board: Study on in circuit Emulators, cross compilers, debuggers | CO5 | Apply |
| 7 | VHDL Programming in FPGA processors | CO4 | Apply |
| 8 | Verilog HDL Programming in FPGA processors | CO3 | Apply |
| 9 | Programming & Simulation in Simulators /Tools/others-ORCAD | CO4 | Analyze |
| 10 | Programming & Simulation in Simulators/Tools/others-MATLAB | CO4 | Analyze |

**Total Periods: 40 periods**

| **Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **POs** | | | | | | | | | | | | **PSOs** | | |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **1** | **2** | **3** |
| **CO1** | 3 | 2 | | | | | | | | | | 2 | | | |
| **CO2** | 3 | 2 | | | | | | | | | | 2 | | | |
| **CO3** | 3 | 2 | | | | | | | | | | 2 | | | |
| **CO4** | 3 | 2 | | | | | | | | | | 2 | | | |
| **CO5** | 3 | 2 | | | | | | | | | | 2 | | | |
| | **3** | **High** | | | | **2** | **Medium** | | | | | **1** | **Low** | | |

| **Summative assessment based on Continuous and End Semester Examination** | | |
|---|---|---|
| **Bloom's Level** | **Internal Assessment [50 marks]** | **End Semester Examination [50 marks]** |
| Remember | 20 | 20 |
| Understand | 10 | 10 |
| Apply | 40 | 40 |
| Analyze | 30 | 30 |
| Evaluate | | |
| Create | | |

**II SEMESTER**

| 22PES201 | REAL TIME OPERATING SYSTEMS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 2 | 0 | 4 |
| **Nature of Course** | Professional Core | | | | |
| **Pre requisites** | Embedded System | | | | |

**Course Objectives**

**The course is intended to**

1. To expose the students to the fundamentals of interaction of OS with a computer and User computation.
2. To teach the fundamental concepts of how process are created and controlled with OS.
3. To study on programming logic of modeling Process based on range of OS features
4. To compare types and Functionalities in commercial OS, application development using RTOS
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| CO1 | Real-time scheduling and schedule ability analysis, including clock-driven and priority-driven scheduling | Analyze |
| CO2 | Theoretical background (specification/verification) and practical knowledge of real-time operating systems. | Apply |
| CO3 | understand the fundamental concepts of real-time operating systems | Apply |
| CO4 | After completing the course students will appreciate the use of multitasking techniques in real- time systems. | Analyze |
| CO5 | Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systems design. | Apply |

**Course Contents:**

**UNITI REVIEW OF OPERATING SYSTEMS 9**

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Introduction to Distributed operating system – issues in distributed system: states, events, clocks-Distributed scheduling-Fault &recovery.

**UNITII OVERVIEW OF RTOS 9**

RTOS Task and Task state -Multithreaded Preemptive scheduler- Process synchronisation- Message queues- Mail boxes -pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks

**UNITIII REAL TIME MODELS AND LANGUAGES 9**

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

**UNITIV REALTIMEKERNEL 9**

Principles – Design issues – RTOS Porting to a Target – Comparison and Basic study of various RTOS like – VX works – Linux supportive RTOS – C Executive.

**UNITV INTRODUCTION TOEMBEDDEDOS 9**

Discussions on Basics of Linux supportive RTOS – UCOS-C Executive for development of RTOS Application -introduction to Android Environment -The Stack – Android User Interface – Preferences, the File System, the Options Menu and Intents, with one Case study.

**TOTAL : 45 PERIODS**

**REFERENCE BOOKS**


1. Silberschatz,Galvin,Gagne" Operating System Concepts,6th edition,JohnWiley,2013
2. Charles Crowley, "Operating Systems-A Design Oriented approach" McGrawHill,2016
3. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill,2009.
4. Karim Yaghmour,Building Embedded Linux System",O'ReillyPub,2003
5. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill,1997.
6. Marko Gargenta,"Learning Android ",O'Reilly2011.
7. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic,1997.
8. Corbet Rubini, Kroah-Hartman, "Linux Device Drivers", O'Reilly,2016.
9. Mukesh Sighal and N G Shi "Advanced Concepts in Operating System", McGrawHill,2000.
10. D.M.Dhamdhere," Operating Systems,A Concept-BasedApproch,TMH,2008.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | | | | | | | | | | 2 | | | |
| CO2 | 3 | 3 | | | | | | | | | | 2 | | | |
| CO3 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO4 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO5 | 3 | 2 | | | | | | | | | | 2 | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PES202 | PYTHON PROGRAMMING WITH MACHINE LEARNING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Basic of Python | | | | |

**Course Objectives**

**The course is intended to**

1. Students will learn the grammar of Python programming language.
2. Students will understand and be able to use the basic programming principles such as data types, variable, conditionals, loops, recursion and function calls.
3. Students will learn how to use basic data structures such as List, Dictionary and be able to manipulate text files and images.
4. Students will understand the process and will acquire skills necessary to effectively attempt a programming problem and implement it with a specific programming language - Python.
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Students will be able to develop skill in system administration | Apply |
| **CO2** | Students will be able to network programming by learningPython | Apply |
| **CO3** | Students will also learn how to effectively use Python's very powerful processing primitives, modeling etc. | Apply |
| **CO4** | Improved Employability and entrepreneurship capacity | Analyze |
| **CO5** | To knowledge up gradation on recent trends in embedded systemsdesign | Analyze |

**Course Contents:**

**UNIT I INTRODUCTION TOPYTHON 9**

Introduction to Python language – Using the interpreter – Python data types and functions – Working with Data – List, Dictionary and Set – Processing Primitives – List comprehensions – File Handling – Object model including Variables, Reference counting, Copying, and Type checking – Error handling.

**UNIT II PROGRAM ORGANIZATION AND FUNCTIONS 9**

Organize Large programs into functions – Python functions including scoping rules and documentation strings – Modules and Libraries – Organize programs into modules – System administration, Text processing, Subprocesses, Binary data handling, XML parsing and Database Access – Installing third-party libraries.

**UNIT III CLASSES AND OBJECTS 9**

Introduction to Object-oriented programming – Basic principles of Object-oriented programming in Python – Class definition, Inheritance, Composition, Operator overloading and Object creation – Python special modules – Python Object System – Object representation, Attribute binding, Memory management, and Special properties of classes including properties, slots and private attributes.

**UNIT IV TESTING, DEBUGGING, AND SOFTWAREDEVELOPMENT PRACTICE 9**

Python Software development – Use of documentation string – Program testing using doctest and Unittest modules – Effective use of assertions – Python debugger and profiler – Iterators and Generators to set up data processing pipelines – An effective technique for addressing common system programming problems (e.g. processing large datafiles, handling infinite data streams, etc.

**UNIT V TEXTI/OHANDLING 9**

Text generation, Template strings and Unicode-packages – Python Integration Primer – Network programming – Accessing C code – Survey on how Python interacts with other language programs.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Mark Lutz,"Learning Python,PowerfulOOPs,O'reilly,2011
2. Robert Sedgewick,Kevin Wayne ,Robert Dondero,Intr Programming in Python,Pearson,2016.
3. Mark J.Guzdial,Barbara Ericson,"Introduction to Computing & Programming in Python,4th Edition Pearson,2015.
4. Budd, Timothy. Exploring Python. McGraw-Hill science,2009.
5. Guttag, John. Introduction to Computation and Programming Using Python. MIT Press,2013.
6. Zelle, John M. Python Programming: An Introduction to Computer Science. 1st ed.Franklin Beedle& Associates,2003.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PES203 | RISC PROCESSOR ARCHITECTURE AND PROGRAMMING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Core | | | | |
| **Pre requisites** | Fundamentals of Basic Microcontroller | | | | |

**Course Objectives**

1. To teach the architecture of general AVRprocessor
2. To teach the architecture and programming of 8/16 bit RISCprocessor
3. To teach the implementation of DSP in ARMprocessor
4. To discuss on memory management, application development in RISCprocessor
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employabilityskills

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| CO1 | Describe the programmer's model of ARM processor and create and test assembly level programming | Apply |
| CO2 | Analyze various types of coprocessors and design suitable co-processor interface to ARM processor. | Analyze |
| CO3 | Identify the architectural support of ARM for operating system and analyze the functionof memory Management unit ofARM | Analyze |
| CO4 | Students will develop more understanding on the concepts ARM Architecture, programming and applicationdevelopment | Apply |
| CO5 | The learning process delivers insight into various embedded processors of RISC architecture / computational processors with improved design strategies. | Apply |

**Course Contents:**

**UNIT I AVR MICROCONTROLLER ARCHITECTURE 12**

Architecture – memory organization – addressing modes – I/O Memory – EEPROM – I/O Ports – SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing

**UNITII ARM ARCHITECTUREANDPROGRAMMING 12**

Arcon RISC Machine – Architectural Inheritance – Core & Architectures -- The ARM Programmer's model -Registers – Pipeline - Interrupts – ARM organization - ARM processor family – Co-processors. Instruction set – Thumb instruction set – Instruction cycle timings

**UNITIII ARMAPPLICATIONDEVELOPMENT 12**

Introduction to RT implementation with ARM – -Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader – Free RTOS Embedded Operating Systems concepts – example on ARM core like ARM9 processor

**UNITIV MEMORY PROTECTION AND MANAGEMENT 12**

Protected Regions-Initializing MPU, Cache and Write Buffer-MPU to MMU-Virtual Memory-Page Tables-TLB-Domain and Memory Access Permission-Fast Context Switch Extension. linear programming, Interior penalty function method, external penalty functionmethod.

**UNITV DESIGN WITH ARMMICROCONTROLLERS 12**

Assembler Rules and Directives- Simple ASM/C programs- Hamming Code- Division-Negation-Simple Loops –Look up table- Block copy- subroutines-application.

**TOTAL : 45 PERIODS**

**REFERENCES**


1. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield 'ARMSystem Developer's Guide Designing and Optimizing System Software', Elsevier2007.
2. Muhammad Ali Mazidi, Sarmad Naimi ,SepehrNaimi' AVR Microcontroller and Embedded Systems using Assembly and C", Pearson Education2014.
3. ARM Architecture Reference Manual, LPC213x UserManual.
4. www.Nuvoton .com/websites on Advanced ARM CortexProcessors.
5. Trevor Martin, 'The Insider's Guide To The Philips ARM7-BasedMicrocontrollers,
6. An Engineer's Introduction To The LPC2100 Series' Hitex (UK)Ltd.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 2 | 3 | | | | | | | | | | 1 | | | |
| CO2 | 3 | 3 | | | | | | | | | | 1 | | | |
| CO3 | 2 | 3 | | | | | | | | | | 1 | | | |
| CO4 | 3 | 2 | | | | | | | | | | 1 | | | |
| CO5 | 3 | 3 | | | | | | | | | | 1 | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom / Online Quiz/Group discussion | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | **(60)** |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

Passed in Board of Studies Meeting (24.02.2022) Approved in Academic Council Meeting (09.03.2022)

Chairman – Board of Studies

| 22PES204 | INTERNET OF THINGS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Core | | | | |
| **Pre requisites** | Fundamentals of Electronics | | | | |

**Course Objectives**

**The course is intended to**

1. To Study about Internet of Things technologies
2. Its role in real time applications
3. To familiarize the accessories and communication techniques for IOT.
4. To familiarize the different platforms
5. Attributes for IOT

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Students will develop more understanding on the concepts of IOT and its present developments. | Apply |
| **CO2** | Students will study about different IOT technologies. | Apply |
| **CO3** | Students will acquire knowledge about different platforms and Infrastructure for IOT | Analyze |
| **CO4** | Students will learn the art of implementing IOT | Apply |
| **CO5** | Students will learn the smart applications and control | Apply |

**Course Contents**

**UNITI INTRODUCTION TO INTERNET OF THINGS 9**

Overview, Technology drivers, Business drivers, Typical IoT applications, Trends and implications

**UNITII IOT ARCHITECTURE 9**

Node Structure - Sensing, Processing, Communication, Powering, Networking - Topologies, Layer/Stack architecture, IoT standards,Cloud computing for IoT,Bluetooth, Bluetooth Low Energy, beacons.

**UNITIII PROTOCOLS AND WIRELESS TECHNOLOGYFORIOT 9**

Protocols: NFC,RFID,Zigbee MIPI, M-PHY, UniPro, SPMI,SPI,M-PCIe Wired vs. Wireless communication,GSM, CDMA, LTE, GPRS, smallcell. Wireless technologies for IoT: WiFi (IEEE 802.11), Bluetooth/Bluetooth Smart, ZigBee/ZigBee Smart, UWB (IEEE 802.15.4), 6LoWPAN, Proprietary systems.

**UNITIV DATA ANALYSTICSFOR IOT 9**

Services/Attributes: Big-Data Analytics and Visualization, Dependability,Security,Maintainability Data analytics for IoT: A framework for data-driven decision making, Descriptive, Predictive and Prescriptive Analytics, Business Intelligence and Artificial Intelligence Importance of impact and open innovation in data-driven decision making.

**UNITV CASE STUDIES 9**

Home Automation, smart cities, Smart Grid, Electric vehicle charging, Environment, Agriculture, Productivity Applications

**TOTAL: 45 PERIODS**

**REFERENCE BOOKS**


1. Arshdeep Bahga and VijaiMadisetti : A Hands-on Approach "Internet ofThings",Universities Press 2018.
2. Oliver Hersent , David Boswarthick and Omar Elloumi " The Internet of Things", Wiley,2016.
3. Samuel Greengard, " The Internet of Things", The MIT press, 2015
4. Adrian McEwen and Hakim Cassimally "Designing the Internet of Things "Wiley,2014.
5. Jean- Philippe Vasseur, Adam Dunkels, "Interconnecting Smart Objects with IP: The Next Internet" Morgan Kuffmann Publishers, 2014.
6. Adrian McEwen and Hakim Cassimally, "Designing the Internet of Things", John Wiley and sons, 2014
7. Lingyang Song/Dusit Niyato/ Zhu Han/ Ekram Hossain," Wireless Device-to-Device Communications and Networks, CAMBRIDGE UNIVERSITY PRESS,2015
8. OvidiuVermesan and Peter Friess (Editors), "Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems", River Publishers Series in Communication, 2013
9. Vijay Madisetti , ArshdeepBahga, "Internet of Things (A Hands on-Approach)", 2014


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 2 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 2 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom / Online Quiz/Group discussion | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PES205 | EMBEDDED SYSTEM LABORATORY-II | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |
| **Nature of Course** | Devices and Circuits | | | | |
| **Pre requisites** | Fundamentals of Embedded Systems | | | | |

**Course Objectives**

**The course is intended to**

1. To study various controllers and different ARM processor.
2. To Learn Programming for Programming Compilers & Platforms on freeware.
3. To Learn Programming with Arduino Microcontroller Board.
4. To learn Simulation Tools as Labview /others
5. To understand the concept of Programming in Python Platform.

**Course Outcomes**

1. The students will learn design with simulators/ex periments,in programming processor boards, processor interfacing/ designing digital controllers.
2. The students will learn design & simulation of Arithmetic ,Logic programs, Filters, Signal analysiswith simulators/ex periments,in programming processor boards, processorint effacing/Tools.
3. The students will learn programming compiling invarious tools & software domains.
4. The students will learn programming compiling in various tools &software domains
5. Learning Communication Protocols & Experimenting with Support Software Tools for communicationinterfaces.

| S.No. | Course Content | CO | Bloom's Level |
|---|---|---|---|
| 1 | Programming ARM processor : ARM7 / ARM9/ARM CortexStudy on incircuit Emulators, crosscompilers, debuggersI/O Programming with ARM processor : ARM7 / ARM9/ARM CortexMicrocontrollers I/O Interfacing : Timers/ Interrupts/ Serial port programming/PWM Generation/ Motor Control/ADC/DAC/ LCD/ RTC Interfacing/ Sensor Interfacing | CO1 | Apply |
| 2 | Programming with Raspberry Pi Microcontroller Board:Study on incircuit Emulators, crosscompilers, debuggers | CO1 | Analyze |
| 3 | I/O Programming with Arduino,Raspberry Pi Microcontroller Boards I/O Interfacing : Timers/ Interrupts/ Serial port programming/PWM Generation/ Motor Control/ADC/DAC/ LCD/ RTC Interfacing/ Sensor Interfacing | CO4 | Apply |
| 4 | Programming with DSP processors | CO2 | Apply |
| 5 | Programming in Freeware softwares/Platforms | CO2 | Apply |
| 6 | Software & Modelling tools<br>✓ Study on MEMSTools<br>✓ Study on process Controllermodeling<br>✓ PLC/SCADA/PCB one type CADTool | CO5 | Analyze |
| 7 | Programming & Simulation in GUI Simulators /Tools/others<br>✓ Graphical User interface simulations & modeling of instrumentation& controllers | CO4 | Apply |
| 8 | Study of one type of Real Time Operating Systems (RTOS) | CO3 | Analyze |
| 9 | Programming & Simulation in Python Simulators/Tools/others | CO4 | Apply |
| 10 | Programming with wired/wireless communication protocol/Network Simulators | CO4 | Apply |

**TOTAL : 40 periods**

**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO2 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO3 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO4 | 3 | 2 | | | | | | | | | | 2 | | | |
| CO5 | 3 | 2 | | | | | | | | | | 2 | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Summative assessment based on Continuous and End Semester Examination | | |
|---|---|---|
| **Bloom's Level** | **Internal Assessment [50 marks]** | **End Semester Examination [50 marks]** |
| Remember | 10 | 10 |
| Understand | | |
| Apply | 50 | 50 |
| Analyze | 40 | 40 |
| Evaluate | | |
| Create | | |

**LIST OF PROFESSIONAL ELECTIVES**

**SEMESTER-I**

| 22PESE01 | ASIC and FPGA Design | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Fundamentals of multiprocessor and multicomputersystems & Architecture | | | | |

**Course Objectives**

**The course is intended to**

1. To study the design flow of different types of ASIC.
2. To familiarize the different types of programming technologies and logic devices.
3. To learn the architecture of different types of FPGA.
4. To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC
5. To analyze the synthesis, Simulation and testing of systems.

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | An ability to understand the operations of multiprocessor and multicomputer systems | Apply |
| **CO2** | Summarizing the various advanced processor technology, pipelining and scalable architectures | Apply |
| **CO3** | Explain the working of superscalar pipeline, cache memory organization | Analyze |
| **CO4** | Comparing the principles of multithreading, multithread architecture, static and dynamic data flow. | Apply |
| **CO5** | Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systemsdesign | Apply |

**Course Contents:**

**UNIT I OVERVIEW OF ASIC AND PLD 9**

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

**UNIT II ASIC PHYSICAL DESIGN 9**

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC

**UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9**

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

**UNIT IV FPGA 9**

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance Case studies: Altera MAX 5000 and 7000 - Altera MAX 9000 – Spartan II and Virtex II FPGAs - Apex and Cyclone FPGAs.

**UNIT V SOC DESIGN 9**

Design Methodologies – Processes and Flows - Embedded software development for SOC – Techniques for SOC Testing – Configurable SOC – Hardware / Software co-design Case studies: Digital camera, Bluetooth radio / modem, SDRAM and USB

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc. 2019
2. S. Trimberger, Field Programmable Gate Array Technology, Edr, Kluwer Academic Publications, 2018.
3. John V.Oldfield, Richard C Dore, Field Programmable Gate Arrays, Wiley Publications 2001.
4. P.K.Chan& S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
5. Parag.K.Lala, Digital System Design using Programmable Logic Devices , BSP, 2003.
6. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin,1992.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 2 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 2 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 2 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

**Formative assessment**

| Bloom's Level | Assessment Component | Marks | Total marks |
|---|---|---|---|
| Remember | Classroom / Online Quiz/Group discussion | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

**Summative Assessment**

| Bloom's Category | Continuous Assessment Tests | | | Terminal Examination (60) |
|---|---|---|---|---|
| | IAE 1 (7.5) | IAE 2 (7.5) | IAE 3 (10) | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PESE02 | ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Fundamentals of multiprocessor and multicomputersystems &Architecture | | | | |

**Course Objectives**

**The course is intended to**

1. To educate the students to the fundamentals of parallel processing
2. To teach the fundamentals of network topologies for multiprocessors
3. To introduce different pipeline designs
4. To introduce features of parallel processors , memory technologies, OS for multiprogrammed computer
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills.

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | An ability to understand the operations of multiprocessor and multicomputer systems | Analyze |
| **CO2** | Summarizing the various advanced processor technology, pipelining and scalable architectures | Analyze |
| **CO3** | Comparing the working of superscalar pipeline, cache memory organization | Apply |
| **CO4** | Classifying the principles of multithreading, multithread architecture, static and dynamic data flow. | Apply |
| **CO5** | Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systemsdesign | Apply |

**Course contents:**

**UNITI THEORYOFPARALLELISM 9**

Parallel Computer models – the state of computing-introduction to parallel processing- parallelism in uni- processors &Multiprocessors -parallel architectural classification schemes-speedup performance laws- -Program and Network Properties-H/W-S/W Parallelism training-applications.

**UNITII SYSTEMINTERCONNECTARCHITECTURES 9**

System interconnect Architectures-Network Properties and routing-Static Interconnection Networks-Dynamic Interconnection Networks-Multiprocessor System Interconnects-inter processor communication network-Structure of Parallel Computers; Hierarchical bus systems-Crossbar switch and multiport memory-multistage and combining network.

**UNITIII PIPELINING ANDSUPERSCALARTECHNOLOGIES 9**

Pipeline principle and implementation-classification of pipeline processor-introduction of arithmetic, instruction, processor pipelining-pipeline mechanisms-hazards

**UNITIV HARDWARE TECHNOLOGIES 9**

Introduction to features of advanced embedded processors through Basic Comparative study :of Architectures -addressing modes -instruction types-performance of- Parallel and scalable architectures, Multiprocessor and SIMD ,MIMD computers, RISC, CISC, Superscalar, VLIW , Vector, Systolic processors of their unique features -Scalable, Multithreaded and data flow Architectures-inter PE communication-interconnection networks- Array & vector processors, vector instruction types- performance modeling-design of vector sing compiler- case Architecture of Itanium processor, Pentium Processor, SPARC Processor.

**UNITV OS ISSUES FOR MULTI PROCESSOR 9**

Introduction-Need for Preemptive OS - Synchronizing and Scheduling in Multiprocessor OS-, Usual OS scheduling Techniques, threads - Classification of multi-processor OS - Software requirements of multiprocessor OS, Distributed scheduler - PVM - PT Threads in shared memory systems.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Kai Hwang "Advanced Computer Architecture".Tata McGraw Hill2018.
2. Advanced Computer architecture , By Rajiv Chopra, S Chand ,2010.
3. JohnL.Hennessy,DavidA.Petterson,"ComputerArchitecture:A Quantitative Approach", 4th Edition, Elsevier,2010
4. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced computer Architecture – A design Space Approach". Pearson Education,2003.
5. Sajjan G. Shiva "Advanced Computer Architecture", Taylor & Francis,2008
6. Rajaraman, C.Siva Ram Murthy, "Parallel Computers- Architecture and Programming",Prentice Hall India,2008
7. Carl Homacher, ZvonkoVranesic, SefwatZaky, "Computer Organisation", 5th Edition,2002.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PESE03 | DIGITAL INSTRUMENTATION | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Fundamentals of Digital Electronics | | | | |

**Course Objectives**

**The course is intended to**

1. To discuss to the students on the fundamentals building blocks of a digital instrument
2. To teach the digital data communication techniques
3. To study on bus communication standards and working principles
4. To teach Graphical programming using GUI for instrument building
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Use digital integrated circuit logic family chips | Apply |
| **CO2** | Perform computational and measurement activities using digital techniques, build sequential and combinational logiccircuits | Analyze |
| **CO3** | Analyse working of A/D and D/A converters, use display devices for digital circuits, use digital meters formeasurements | Analyze |
| **CO4** | Graduates will understand the fundamental principles of electrical and electronics circuits and instrumentation, enabling them to understand current technology and to adapt to new devices and technologies. | Apply |
| **CO5** | Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systemsdesign | Apply |

**Course Contents:**

**UNITI DATA ACQUISITION SYSTEMS 9**

Overview of A/D converter, types and characteristics – Sampling, Errors. Objective – Building blocks of Automation systems -Calibration, Resolution, Data acquisition interface requirements – Counters – Modes of operation- Frequency, Period, Time interval measurements, Prescaler, Heterodyne converter for frequency measurement, Single and Multi-channel Data Acquisition systems-Digital storage Oscilloscope-digital displayinterface.

**UNITII INSTRUMENT COMMUNICATION 9**

Introduction, Modem standards, Data transmission systems- Time Division Multiplexing (TDM) – Digital Modulation Basic requirements of Instrument Bus Communications standards, interrupt and data handshaking ,serial bus- basics, Message transfer, - RS-232, USB, RS-422, Ethernet Bus-CAN standards interfaces .General considerations -advantages and disadvantages-Instrumentation network design ,advantages and limitations ,general considerations, architecture, model, and system configuration of : HART network, Mod Bus,Field bus.

**UNITIII VIRTUALINSTRUMENTATION BASICS 9**

Block diagram, role, and Architecture for VI— tool bar, Graphical system design &programming using GUI - Virtual Instrumentation for test, control design-modular programming-conceptual and prog approaches for creation of panels, icons-Loops-Arrays-clusters-plotting data-structures-strings and File I/O- Instrument Drivers.

**UNITIV CONFIGURING PROGRAMMABLE INSTRUMENTATION 9**

Microprocessor based system design -Peripheral Interfaces systems and instrument communication standards -Data acquisition with processor and with VI - Virtual Instrumentation Software and hardware simulation of I/O communication blocks-peripheral interface - ADC/DAC - Digital I/O – Counter , Timer-servo motor control-PID control.

**UNITV CASE STUDIES** **9**

Processor based DAS, Data loggers, VI based process measurements like temperature, pressure and level development system- DSO interface -digital controller for colour video display.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1.Mathivanan, "PC based Instrumentation Concepts and practice", Prentice-Hall India, 2009
2.Jovitha Jerome,"Virtual Instrumentation using Labview"PHI,2010.
3. Gregory J. Pottie / William J. Kaiser, Principles Of Embedded Networked Systems Design,CAMBRIDGE UNIVERSITY PRESS (CUP),2016
4.Jonathan W Valvano, "Embedded Microcomputer systems", Brooks/Cole, Thomson, 2010.
5.Cory L.Clark,"Labview Digital Signal Processing & Digital Communication,TMcH,2005
6.Lisa K. wells & Jeffrey Travis, Lab VIEW for everyone, Prentice Hall, New Jersey,1997.
7.S Kalsi, "Electronic Instrumentation" Second Edition, Tata McGraw-Hill,2006.
8.K.Padmanabhan, S.Ananthi A Treatise on Instrumentation Engineering ,I K Publish,2011
9.Gary Johnson, LabVIEW Graphical Programming, Second edition, McGHill,Newyork, 1997.

**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

**LIST OF PROFESSIONAL ELECTIVES**

**SEMESTER-II**

| 22PESE11 | DEVICE DRIVER EMBEDDEDLINUX | L | P | T | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | fundamentals of Linux Operating system | | | | |

**Course Objectives**

**The course is intended to**

1. To expose the students to the fundamentals of Linux Operating system, its basic commands and shell programming
2. To teach the history of embedded Linux, various distributions and basics of GNU Cross Platform ToolChain.
3. To study on different Host-Target setup, debug and various memory device, file systems and performance tuning.
4. To introduce the concept of configuring kernel using the cross-platform toolchain.
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employabilityskills

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Executing Linux desktop and GNU tool chain with Eclipse IDE | Apply |
| **CO2** | Finding cross compile Linux kernel and port it to targetboard | Analyze |
| **CO3** | Add applications and write customized application for the Linux kernel in the targetboard | Apply |
| **CO4** | . Students will study about distributions and cross platform tool chain. | Apply |
| **CO5** | Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systems design | Apply |

**Course Contents:**

**UNITI FUNDAMENTALSOFLINUX 9**

Basic Linux System Concepts: Working with Files and Directories - Introduction to Linux File system - Working with Partitions and File systems - Understanding Linux Permissions; Using Command Line Tools: Executing Commands from the Command Line - Getting to a Shell - Popular Command-Line Commands - Working with the Bash Shell.

**UNITII VARIOUS DISTRIBUTIONS AND CROSS PLATFORMTOOLCHAIN 9**

Introduction - History of Embedded Linux - Embedded Linux versus Desktop Linux - Commercial Embedded Linux Distribution - Choosing a distribution - Embedded Linux Distributions - Architecture of Embedded Linux - Linux Kernel Architecture - Porting Roadmap - GNU Cross Platform Toolchain

**UNITIII HOST-TARGET SETUP ANDOVERALLARCHITECTURE 9**

Real Life Embedded Linux Systems - Design and Implementation Methodology - Types of Host/Target Development Setups - Types of Host/Target Debug Setups - Generic Architecture of an Embedded Linux System - System Startup - Types of Boot Configurations - System Memory Layout - Processor Architectures - Buses and Interfaces - I/O – Storage.

**UNITIV KERNELCONFIGURATION 9**

A Practical Project Workspace - GNU Cross-Platform Development Toolchain - C Library Alternatives-Other Programming Languages - Eclipse: An Integrated Development Environment -

Terminal Emulators - Selecting a Kernel - Configuring the Kernel - Compiling the Kernel - Installing the Kernel - Basic Root Filesystem Structure - Libraries - Kernel Modules and Kernel Images - Device Files - Main System Applications - System Initialization.

**UNITV LINUX DRIVERS 9**

Introduction in to basics on Linux drivers, introduction to GNU cross platform Toolchain- Case study on programming one serial driver for developing application using LinuxDriver

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum, 'Building Embedded Linux Systems 2nd Edition', SPD -O'Reilly Publications,2008
2. P.Raghavan,Amol Lad,Sriram Neelakandan,"EmbeddedLinux System Design &Development,Auerbach Publications,2012
3. William von Hagen, 'Ubuntu Linux Bible 3rd Edition', Wiley Publishing Inc.,2010
4. Jonathan Corbet, Alessandro Rubini & Greg Kroah-Hartman, 'Linux Device Drivers 3rd Edition', SPD -O'Reilly Publications,2011
5. Robert Love,"Linux System Programming, SPD -O'Reilly Publications,2010


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

Passed in Board of Studies Meeting (24.02.2022) Approved in Academic Council Meeting (09.03.2022)

Chairman – Board of Studies

| 22PESE12 | ADVANCED DIGITAL SIGNAL PROCESSORS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | fundamentals of digital signal processing | | | | |

**Course Objectives**

**The course is intended to**

1. To expose the students to the fundamentals of digital signal processing in frequency domain& its application
2. To teach the fundamentals of digital signal processing in time-frequency domain& its application
3. To compare Architectures & features of Programmable DSprocessors & develop logical functions of DSProcessors
4. To discuss on Application development with commercial family of DSProcessors
5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills.

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Students will learn the essential advanced topics in DSP that are necessary for successful Postgraduate level research | Apply |
| **CO2** | Students will have the ability to solve various types of practical problems in DSP | Apply |
| **CO3** | Comprehend the DFTs and FFTs, design and Analyze the digital filters, comprehend the Finite word length effects in Fixed point DSP Systems | Analyze |
| **CO4** | . The conceptual aspects of Signal processing Transforms areintroduced | Apply |
| **CO5** | Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systemsdesign | Apply |

**Course Contents:**

**UNITI FUNDAMENTALS OFDSP 9**

Frequency interpretation, sampling theorem, aliasing, discrete-time systems, constant-coefficient difference equation. Digital filters: FIR filter design – rectangular, Hamming,Hanning windowing technique. IIR filter design – Butterworth filter, bilinear transformation method, frequency transformation. Fundamentals of multirate processing – decimation and interpolation

**UNITII TRANSFORMSANDPROPERTIES 9**

Discrete Fourier transform (DFT): - properties, Fast Fourier transform (FFT), DIT-FFT, and DIF-FFT. Wavelet transforms:Introduction, wavelet coefficients – orthonormal wavelets and their relationship to filter banks, multi-resolution analysis, and Haar and Daubechies wavelet

**UNITIII ADAPTIVE FILTERS 9**

Wiener filters – an introduction. Adaptive filters: Fundamentals of adaptive filters, FIR adaptive filter – steepest descent algorithm, LMS algorithm, NLMS, applications – channel equalization. Adaptive recursive filters – exponentially weighted RLS algorithm

**UNITIV ARCHITECTURE OF COMMERCIAL DIGITAL SIGNAL PROCESSORS 9**

Introduction to commercial digital signal processors, Categorization of DSP processor – Fixed point and floating point, Architecture and instruction set of the TI TMS 320 C54xx and TMS 320 C6xxx DSP processors, On-chip and On-board peripherals – memory (Cache, Flash, SDRAM), codec, multichannel buffered I/O serial ports (McBSPs), interrupts, direct memory access (DMA), timers and general purpose I/Os.

**UNITV INTERFACING I/O PERIPHERALS FOR DSPBASEDAPPLICATIONS 9**

Introduction, External Bus Interfacing Signals, Memory Interface, I/O Interface, Programmed I/O, Interrupts, Design of Filter, FFT Algorithm, ,Application for Serial Interfacing, DSP based Power Meter, Position control , CODEC Interface.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. John. G. Proakis, Dimitris G. Manolakis, "Digital signal processing", Pearson Edu,2012
2. Sen M.Kuo,Woon-Seng S.Gan, "Digital Signal Processors- Pearson Edu,2012
3. Ifeachor E. C., Jervis B. W ,"Digital Signal Processing: A practical approach, Pearson-Education, PHI/2002
4. Shaila D. Apte, " Digital Signal Processing", Second Edition, Wiley,2016.
5. Robert J.Schilling,Sandra L.Harris,"Introd. To Digital Signal Processing with Matlab",Cengage,2014.
6. Steven A. Tretter, "Communication System Design Using DSP Algorithms with Laboratory Experiments for the TMS320C6713™ DSK", Springer,2008.
7. RulphChassaing and Donald Reay, "Digital Signal Processing and Applications with the TMS320C6713 and TMS320C6416 DSK", John Wiley & Sons, Inc., Hoboken, New Jersey, 2008.
8. K.P. Soman and K.L. Ramchandran,Insight into WAVELETS from theory to practice, Eastern Economy Edition,2008
9. B Venkataramani and M Bhaskar "Digital Signal Processors", TMH, 2nd,2010
10. Vinay K.Ingle,John G.Proakis,"DSP-A Matlab Based Approach",CengageLearning,2010
11. Taan S.Elali,"Discrete Systems and Digital Signal Processing with Matlab",CRCPress2009.
12. Monson H. Hayes, "Statistical Digital signal processing and modelling", John Wiley & Sons, 2008.
13. AvatarSing, S. Srinivasan, "Digital Signal Processing- Implementation using DSP Microprocessors with Examples from TMS320C54xx", ThomsonIndia,2004


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| **Formative assessment** | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| **Summative Assessment** | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | **(60)** |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 20PESE13 | EMBEDDED AND REAL TIME SYSTEMS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Embedded System | | | | |

**Course Objectives**

**The course is intended to**

1. Understand the basic concepts of embedded systems.
2. Articulate Embedded Programs for simple applications.
3. Deduce the testing methodologies of hardware and software tools.
4. Represent the basic knowledge on embedded systems with real time systems.
5. Express embedded systems knowledge with respect to communication field

**Course Outcomes**

On successful completion of the course the students will be able to

| CO. No | Course Outcome | Bloom's Level |
|---|---|---|
| CO 1 | Infer a system component, or process to meet desiredneeds within realistic constraints such as economic, environmental, social, political, and ethical. | Understand |
| CO 2 | Construct simple programs on embedded platforms. | Apply |
| CO 3 | Correlate design and test systems that include both Hardware and software. | Analyze |
| CO 4 | Interpret knowledge on embedded systems with real time applications. | Understand |
| CO 5 | Describe the knowledge in embedded systems with respect to communication field | Understand |

**Course Contents**

**UNIT I INTRODUCTION TO EMBEDDED SYSTEMS 9**

Introduction to Embedded Systems -Structural units in Embedded processor, selection of processor & memory devices- DMA, Memory management methods- memory mapping, cache replacement concept, Timer and Counting devices, Watchdog Timer, Real Time Clock

**UNIT II SYSTEM MODELLING WITH HARDWARE / SOFTWARE PARTITIONING 9**

Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modelling- Single- processor Architectures &,Multi-Processor Architectures, comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modelling, Formulation of the HW/SW scheduling, Optimization.

**UNIT III HARDWARE /SOFTWARE CO-SYNTHESIS 9**

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

**UNIT IV REAL TIME DATABASES 9**

Real time databases -Basic definition, Real time Vs General purpose databases, Main memory databases, Transaction priorities, Transaction aborts, Concurrency control issues, Disk scheduling algorithms, two -phase approach to improve predictability -Maintaining serialization consistency.

**UNIT V REAL TIME COMMUNICATION** **9**

Real -time communication -Communications media, Network topologies protocols, Fault tolerant Routing. Fault tolerance techniques -Fault types -Fault detection. Fault error containment Redundancy -Data diversity -Reversal checks -Integrated failure handling.

**Total : 45 Periods**

**Text Books:**


1. Rajkamal, 'Embedded system-Architecture, Programming, Design', Tata McGraw Hill, 2019.
2. Shibu.K.V, "Introduction to Embedded Systems", Tata McGraw Hill,2018
3. Jonathan W.Valvano,"Embedded Microcomputer Systems ,Real Time Interfacing", Cengage Learning,3rd edition,2012


**Reference Books:**


1. Peckol, "Embedded system Design",JohnWiley&Sons,2010
2. Rajib Mall, ‖Real-time systems: theory and practice‖, Pearson Education, 2007.
3. R.J.A Buhur and D.L Bailey, ¯An Introduction to Real -Time Systems‖, Prentice -Hall International, 1999.
4. Peter D. Lawrence, ¯ Real Time Micro Computer System Design - An Introduction ‖, Tata McGraw Hill, 1998.


**Additional References**

1. **NPTEL -** https://nptel.ac.in/courses/108/102/108102045/
2. **MOOC Courses -** https://www.mooc-list.com/tags/embedded-systems

| Mapping of Course Outcomes (COs) with Programme Outcomes (POs) Programme Specific Outcomes (PSOs) | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **POs** | | | | | | | | | | | | **PSOs** | |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **1** | **2** |
| **CO 1** | 3 | 2 | | | 3 | | | | | | | 2 | | |
| **CO 2** | 3 | 2 | | | 3 | | | | | | | 2 | | |
| **CO 3** | 3 | 2 | | | 3 | | | | | | | 2 | | |
| **CO 4** | 3 | 2 | | | 3 | | | | | | | 2 | | |
| **CO 5** | 3 | 2 | | | 3 | | | | | | | 2 | | |
| | **3-High** | | | | **2-Medium** | | | | **1-Low** | | | | | |

| Formative Assessment | | | |
|---|---|---|---|
| **Blooms Taxonomy** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Quiz | 5 | 15 |
| Understand | Tutorial class / Assignment | 5 | |
| Apply | | | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Internal Assessment Examinations (IAE)** | | | **Final Examinations (FE)** |
| | **IAE – I (7.5)** | **IAE – II (7.5)** | **IAE – III (10)** | **60** |
| Remember | 10 | 10 | 10 | 20 |
| Understand | 30 | 30 | 30 | 60 |
| Apply | 10 | 10 | 10 | 20 |
| Analyse | | | | |
| Evaluate | | | | |
| Create | | | | |

# Professional Elective III

| 22PESE21 | EMBEDDED PRODUCT DEVELOPMENT | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Basis of Embedded System | | | | |

**Course Objectives**

**The course is intended to**

1. The course aims at providing the basic concepts of product design,
2. Product features and its architecture
3. Student can have a basic knowledge in the common features a product
4. How to incorporate them suitably inproduct.
5. To learn about Embedded Products design.

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Understand the integration of customer requirements in productdesign | Apply |
| **CO2** | Apply structural approach to concept generation, creativity, selection andtesting | Apply |
| **CO3** | Understand various aspects of design such as industrial design, design of Consumer specific product, its Reverse Engineering manufacture | Analyze |
| **CO4** | Interpreting various aspects of design such as industrial design, design ofeconomic analysis and productarchitecture | Apply |
| **CO5** | Implementing Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employabilityskills | Apply |

**Course Contents:**

**UNITI CONCEPTS OFPRODUCTDEVELOPMENT 12**

Need for PD- Generic product Development Process Phases- Product Development Process Flows- Product Development organization structures-Strategic importance of Product Planning process – Product Specifications-Target Specifications-Plan and establish product specifications - integration of customer, designer, material supplier and process planner, Competitor and customer - Understanding customer and behavior analysis. Concept Generation, Five Step Method-Basics of Concept selection- Creative thinking -creativity and problem solving- creative thinking methods- generating design concepts-systematic methods for designing -functional decomposition – physical decomposition.

**UNITII INTRODUCTION TO APPROACHES IN PRODUCTDEVELOPMENT 12**

Product development management - establishing the architecture - creation - Product Architecture changes - variety – component standardization , clustering -geometric layout development - Fundamental and incidental interactions - related system level design issues - secondary systems - architecture of the chunks - creating detailed interface specifications-Portfolio Architecture- competitive benchmarking- Approach for the benchmarking process-Design for manufacturing - Industrial Design-Robust Design – Prototype basics - Principles of prototyping - Planning for prototypes- Economic & Cost Analysis -Testing Methodologies- ProductBranding.

**UNITIII INDUSTRIALDESIGNSTRATEGIES 6**

Role of Integrating CAE, CAD, CAM tools for Simulating product performance and manufacturing processes electronically- Basics on reverse engineering – Reverse engineering strategies – Finding reusable software components – Recycling real-time embedded software based approach and its logical basics- Incorporating reverse engineering for consumer product development -case study on DeskJet Printer.

**UNITIV ELECTRONIC PRODUCTDEVELOPMENTSTAGES 6**

Product Development Stages-Embedded product modeling- Linear, Iterative, Prototyping, Spiral - Selection of Sensor, Voltage Supply, Power supply protection, Grounding and noise elimination

methods, Thermal protection with heat management - PCB design steps - Software design and testing method – documentation.

**UNITV EMBEDDEDPRODUCTSDESIGN 9**

Creating general Embedded System Architecture(with Case study example: Mobile Phone / DeskJet Printer./ Robonoid as a product) -Architectural Structures- Criteria in selection of Hardware & Software Components, processors, input/output interfaces & connectors, ADC System,Memory, choosing Bus Communication Standards, Criteria in selection of Embedded OS/Device Drivers, Need for Developing with IDE, Translation & Debugging Tools & Application Software, Performance Testing, Costing, Benchmarking,Documentation

**TOTAL: 45 PERIODS**

**REFERENCES**


1. Product Design and Development", Anita Goyal, Karl T Ulrich, Steven D Eppinger, McGraw -Hill International Edns.2019/ Tata McGrawEducation, ISBN-10-007-14679-9.
2. R.G. Kaduskar and V.B. Baru, " Electronic Product Design", Wiley, 2014.
3. George E.Dieter, Linda C.Schmidt, "Engineering Design", McGraw-Hill International Edition,4th Edition,2019, ISBN 978-007-127189-9
4. Stephen Armstrong, Engineering and Product Development Management ; The Holistic Approach, CAMBRIDGE UNIVERSITY PRESS (CUP),2014
5. Rajkamal, 'Embedded system-Architecture, Programming, Design', TMH,2015.
6. KEVIN OTTO & KRISTIN WOOD, "Product Design and Development", 4th Edition,2013, Product Design Techniques in Reverse Engineering and New Product Development, , Pearson Education (LPE),2001./ISBN 9788177588217


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

**Formative assessment**

| Bloom's Level | Assessment Component | Marks | Total marks |
|---|---|---|---|
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| **Summative Assessment** | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 2PESE22 | ELECTRIC VEHICLES AND POWER MANAGEMENT | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Power Management System | | | | |

**Course Objectives**

**The course is intended to**

1. To understand the concept of electrical vehicles
2. To understand the concept of the operations
3. To understand the need for energy storage in hybrid vehicles
4. To provide knowledge about various possible energy storage technologies
5. Learners will understand the operation of Electric vehicles and various energy storage Technologies for electrical vehicles.

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Learners will understand the operation of Electric vehicles. | Apply |
| **CO2** | Learners will understand the operation various energy storage technologies for electrical vehicles | Apply |
| **CO3** | Learners will understand the used in electrical vehicles | Apply |
| **CO4** | Design the electrical vehicles | Analyze |
| **CO5** | Discuss the design issues EV. | Apply |

**Course Contents:**

**UNIT I ELECTRIC VEHICLES AND VEHICLE MECHANICS 9**

Electric Vehicles (EV), Hybrid Electric Vehicles (HEV), Engine ratings, Comparisons of EV with internal combustion Engine vehicles, Fundamentals of vehicle mechanics.

**UNIT II ARCHITECTURE OF EV's AND POWER TRAIN COMPONENTS 9**

Architecture of EV's and HEV's - Plug-n Hybrid Electric Vehicles (PHEV)- Power train components and sizing, Gears, Clutches, Transmission and Brakes.

**UNIT III CONTROL OF DC AND AC DRIVES 9**

DC/DC chopper based four quadrant operations of DC drives - Inverter based V/f Operation (Motoring and braking) of induction motor drive system - Induction motor and permanent motor based vector control operation – Switched reluctance motor (SRM) drives.

**UNIT IV BATTERY ENERGY STORAGE SYSTEM 9**

Battery Basics, Different types, Battery Parameters, Battery modeling, Traction Batteries.

**UNITV ALTERNATIVE ENERGY STORAGE SYSTEMS 9**

Fuel cell - Characteristics- Types - hydrogen Storage Systems and Fuel cell EV - Ultra capacitors.

**TOTAL:45 PERIODS**

**REFERENCES**

1. Iqbal Hussain, "Electric and Hybrid Vehicles: Design Fundamentals, Second Edition" CRC Press, Taylor & Francis Group, Second Edition (2011).
2. Ali Emadi, Mehrdad Ehsani, John M.Miller, "Vehicular Electric Power Systems", Special Indian Edition, Marcel dekker, Inc 2010..

| Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **POs** | | | | | | | | | | | | **PSOs** | | |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **1** | **2** | **3** |
| **CO1** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO2** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO3** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO4** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO5** | 3 | 3 | 2 | | | | | | | | | | | | |
| | **3** | **High** | | | | **2** | **Medium** | | | | | **1** | **Low** | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PESE23 | RECONFIGURABLE PROCESSOR AND SOC DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Basic of Reconfigurable Processortechnologies | | | | |

**Course Objectives**

1. To introduce the Reconfigurable Processortechnologies
2. To familiarize the need and role of Reconfigurable Processor
3. Embedded systemapplications.
4. To impart the knowledge of Reconfigurable embedded Processor
5. Real time applications.

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Adaptability, in its complete strength, is present in reconfigurable processors which makes it an important IP in modern System-on-Chips (SoCs) | Analyze |
| **CO2** | Reconfigurable processors have risen to prominence as a dominant computing platform | Analyze |
| **CO3** | Understand various aspects across embedded, general-purpose, and high-performance application domains during the last decade | Analyze |
| **CO4** | Improved Employability and entrepreneurship capacity due to knowledge up gradation | Apply |
| **CO5** | The concepts recent trends in embedded systemsdesign | Analyze |

**Course Contents:**

**UNITI INTRODUCTION 9**

Introduction to reconfigurable processor- Reconfigurable Computing-Programming elements and Programming Tools for Reconfigurable Processors, ASIC design flow- Hardware/Software Co design- FPAA Architecture overview- recent trends in Reconfigurable Processor &SoC.

**UNITII PROGRAMMABLE LOGICDEVICES CPLD 9**

Introduction to Programmable logic devices, SPLDs, CPLD building blocks- Architectures and features of Altera:MAX 7000, MAX V- Xilinx XC 9500,Cool Runner-II.

**UNITIII PROGRAMMABLE LOGICDEVICES FPGA 9**

FPGA architecture overview- Challenges of FPGA processor design-Opportunities of FPGA processor design- Designing Soft-core Processors – Designing Hardcore Processors – hardware/software co simulation- FPGA to multi core embedded computing- FPGA based on-board computer system.

**UNITIV RECONFIGURABLE SOCPROCESSORS 9**

SoC Overview -Architecture and applications of Xilinx Virtex II pro, Zynq-7000, Altera Excalibur, Cyclone V -Triscend A7, E5- Atmel FPSLIC- Multicore SoCs.

**UNITV RECONFIGURABLE PROCESSOR ANDSOCAPPLICATIONS 9**

Reconfigurable processor based DC motor control- digital filter design- mobile phone development- High Speed Data Acquisition -Image Processing application-controller implementation for mobile robot.

**TOTAL:45 PERIODS**

**REFERENCES**


1. Nurmi,Jari(Ed.) "Processor Design System-On-Chip Computing for ASICs and FPGAs" Springer,2017.
2. Ian Grout , “Digital system design with FPGAs and CPLDs” Elsevier,2016.
3. Joao Cardoso, Michael Hübner, "Reconfigurable Computing: From FPGAsto Hardware/Software Codesign" Springer, 2011.
4. Ron Sass and AnderewG.Schmidt, “ Embedded System design with platform FPGAs:

Principles and Practices", Elsevier,2010.
5. Steve Kilts, "Advanced FPGA Design: Architecture, Implementation, and Optimization" Willey, 2007

| Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **POs** | | | | | | | | | | | | **PSOs** | | |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **1** | **2** | **3** |
| **CO1** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO2** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO3** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO4** | 3 | 3 | 2 | | | | | | | | | | | | |
| **CO5** | 3 | 3 | 2 | | | | | | | | | | | | |
| | **3** | **High** | | | | **2** | **Medium** | | | | | **1** | **Low** | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 20 | 20 | 20 | 40 |
| Analyze | 30 | 30 | 30 | 60 |
| Evaluate | | | | |
| Create | | | | |

| 22PESE31 | DIGITAL IMAGE PROCESSING | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Digital Based applications | | | | |

**Course Objectives**

**The course is intended to**

1. the fundamentals of imageprocessing
2. the techniques involved in imageenhancement
3. the low and high-level features for imageanalysis
4. the fundamentals and significance of imagecompression
5. the hardware for image processingapplications

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | Students will develop more understanding on the concepts of smart system design and its presentdevelopments. | Apply |
| **CO2** | Students will study about different embedded open source and cost effective techniques for developing solution for real time applications. | Analyze |
| **CO3** | Students will acquire knowledge on different platforms and Infrastructure for Smart system design. | Apply |
| **CO4** | Improved Employability and entrepreneurship capacity due to knowledge up gradation | Analyze |
| **CO5** | Students will learn the art of implementing embedded system for smart applications and control. | Analyze |

**Course Contents:**

**UNITI FUNDAMENTALS OFIMAGE PROCESSING 9**

Introduction to image processing systems, sampling and quantization, color fundamentals and models, image operations – arithmetic, geometric and morphological. Multi-resolution analysis – imagepyramids.

**UNITII IMAGE ENHANCEMENT 9**

Spatial domain; Gray-level transformations - histogram processing - spatial filtering, smoothing and sharpening. Frequency domain: filtering in frequency domain - DFT, FFT, DCT - smoothing and sharpening filters - Homomorphic filtering. Image enhancement for remote sensing images and medical images.

**UNITIII IMAGE SEGMENTATION ANDFEATUREANALYSIS 9**

Detection of discontinuities - edge operators - edge linking and boundary detection, thresholding - feature analysis and extraction - region based segmentation - morphological watersheds - shape skeletonization, phase congruency. Number plate detection using segmentation algorithm.

**UNITIV IMAGE COMPRESSION 9**

Image compression: fundamentals – models – elements of information theory – error free compression - lossy compression - compression standards. Applications of image compression techniques in video and imagetransmission.

**UNITV EMBEDDED IMAGE PROCESSING 9**

Introduction to embedded image processing. ASIC vs FPGA - memory requirement, power consumption, parallelism. Design issues in VLSI implementation of Image processing algorithms - interfacing. Hardware implementation of image processing algorithms: Segmentation and compression.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Rafael C. Gonzalez and Richard E. Woods, "Digital Image processing", 4nd edition, Pearson education,2019
2. Anil K. Jain, "Fundamentals of digital image processing", Pearson education,2003

3. Milan Sonka, ValclavHalavac and Roger Boyle, “Image processing, analysis and machine vision”, 2nd Edition, Thomson learning,2011
4. Mark Nixon and Alberto Aguado,“Feature extraction & Image processing for computer vision”,3rd Edition, Academic press,2012
5. Donald G. Bailey, “Design for Embedded Image processing on FPGAs” John Wiley and Sons, 2011.

**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom’s Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom’s Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 20 | 20 | 20 | 40 |
| Analyze | 30 | 30 | 30 | 60 |
| Evaluate | | | | |
| Create | | | | |

| 22PESE32 | EMBEDDED NETWORKING AND AUTOMATION OF ELECTRICAL SYSTEM | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Digital Based applications | | | | |

**Course Objectives**

**The course is intended to**

1. The fundamentals of imageprocessing
2. The techniques involved in imageenhancement
3. The low and high-level features for imageanalysis
4. The fundamentals and significance of imagecompression
5. The hardware for image processingapplications

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | The learning process delivers insight into categorizing various i/p-o/p configurations of computational processors with improved communication strategies | Analyze |
| **CO2** | Students will study about different embedded open source and cost effective techniques for developing solution for real time applications. | Apply |
| **CO3** | Students will acquire knowledge on different platforms and Infrastructure for Smart system design. | Analyze |
| **CO4** | Improved Employability and entrepreneurship capacity due to knowledge upgradation on recent trends in embedded systems design. | Apply |
| **CO5** | Students will learn the art of implementing embedded system for smart applications and control. | Apply |

**Course Contents:**

**UNITI EMBEDDED PROCESS COMMUNICATION WITHINSTRUMENTBUS 9**

Embedded Networking: Introduction – Cluster of Instruments in System: introduction to bus protocols, connectors, Bus Architecture & Interfacing of external instruments to – RS 232C,RS – 422, RS 485 and USB standards – embedded Ethernet – MOD bus and CAN bus.

**UNITII WIRELESSEMBEDDEDNETWORKING 9**

Wireless sensor networks – Introduction – Sensor node architecture – Commercially available sensor nodes -Network Topology -Localization -Time Synchronization - Energy efficient MAC protocols – SMAC -Energy efficient and robust routing – Data Centric routing Applications of sensor networks; Applications - Home Control - Building Automation - Industrial Automation.

**UNITIII BUILDINGSYSTEM AUTOMATION 9**

Concept of Uc Based & PC based data acquisition – Concept of Virtual Instrumentation - Programming Environment to build a Virtual Instrumentation, Building system automation with graphical user interface programming-Programmable Logic Controllers-introduction-Ladder& Functional Block programming-Case study on Temperature control, Valve sequencingcontrol.

**UNITIV MEASUREMENT AND EMBEDDED CONTROL OFELECTRICALAPPARATUS 9**

Sensor Types & Characteristics : Sensing Voltage, Current, flux, Torque, Position, Proximity, Force, Data acquisition & Display system- Signal conditioning circuit design- computers/ embedded processor interfacing circuit -design automation and protection of electrical appliances -processor based digital controllers for switching Actuators: Servo motors, Stepper motors,Relays

**UNITV COMMUNICATION FOR LARGE ELECTRICALSYSTEMAUTOMATION 9**

Data Acquisition, Monitoring, Communication, Event Processing, and Polling Principles, SCADA

system principles – outage management- Decision support application for substation automation,

extended control feeder automation, Performance measure and response time, SCADA Data Models, need, sources, interface.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. Control and automation of electrical power distribution systems, James Northcote-Green, Robert Wilson, CRC, Taylor and Francis,2006
2. Krzysztof Iniewski,"Smart Grid ,Infrastructure &Networking",TMcGH,2012
3. Robert Faludi,"Building Wireless SensorNetworks,O'Reilly,2011
4. W.Bolton,Programmable Logic Controllers,5thEd,Elseiver,2010.
5. Shih-Lin Wu,Yu-Chee Tseng,{"Wireless Ad Hoc Networking,PAN,LAN,SAN,AurebachPub,2012
6. Jan Axelson 'Embedded Ethernet and Internet Complete', Penrampublications
7. Bhaskar Krishnamachari, 'Networking wireless sensors', Cambridge press2005
8. Robert H. Bishop, "Learning with Lab-View" Preticee Hall, 2009
9. Sanjay Gupta, "Virtual Instrumentation, LABVIEW", TMH, New Delhi,2003
10. Ernest O. Doeblin and Dhanesh N Manik, " Measrement Systems – Application and Design", 5th Edn, TMH, 2007.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

**Formative assessment**

| Bloom's Level | Assessment Component | Marks | Total marks |
|---|---|---|---|
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

**Summative Assessment**

| Bloom's Category | Continuous Assessment Tests | | | Terminal Examination (60) |
|---|---|---|---|---|
| | IAE 1 (7.5) | IAE 2 (7.5) | IAE 3 (10) | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |

| 22PESE33 | SMART SYSTEM DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| **Nature of Course** | Professional Elective | | | | |
| **Pre requisites** | Digital Electronics Based applications | | | | |

**Course Objectives**

**The course is intended to**

1. To understand about the smart system technologies and its role in real timeapplications
2. To expose students to different open source platforms andAttributes.
3. To familiarize the design and development of embedded system based systemdesign.
4. To knowledge upgradation on recent trends in embedded systems design .
5. To learn the art of implementing embedded system for smart applications and control

**Course Outcomes**

On successful completion of the course, students will be able to

| CO.No. | Course Outcome | Bloom's Level |
|---|---|---|
| **CO1** | The learning process delivers insight into categorizing various i/p-o/p configurations of computational processors with improved communication strategies | Apply |
| **CO2** | Students will study about different embedded open source and cost effective techniques for developing solution for real time applications. | Apply |
| **CO3** | Students will acquire knowledge on different platforms and Infrastructure for Smart system design. | Analyze |
| **CO4** | Improved Employability and entrepreneurship capacity due to knowledge upgradation on recent trends in embedded systems design. | Apply |
| **CO5** | Students will learn the art of implementing embedded system for smart applications and control. | Apply |

**Course content:**

**UNITI INTRODUCTION 9**

Overview of smart system design and requirements- Hardware and software selection & co-design-Communications-smart sensors and actuators-Open-source resources for embedded system-android for embedded system - Embedded system for Ecommerce- Embedded system for Smart card design and development –Recent trends.

**UNITII MOBILEEMBEDDEDSYSTEM 9**

Design requirements-Hardware platform- OS and Software development platform- Mobile Apps development- Applications: heart beat monitoring, blood pressure monitoring, mobile banking and appliances control.

**UNITIII HOMEAUTOMATION 9**

Home Automation System Architecture-Essential Components- Linux and Raspberry Pi – design and real time implementation.

**UNITIV SMART APPLIANCES ANDENERGYMANAGEMENT 9**

Overview- functional requirements-Embedded and Integrated Platforms for Energy Management-Energy Measurement Techniques for Smart Metering-Smart Embedded Appliances Networks – Security Considerations.

**UNITV EMBEDDED SYSTEMSANDROBOTICS 9**

Robots and Controllers-components - Aerial Robotics -Mobile Robot Design- Three-Servo Ant Robot- Autonomous Hexacopter System.

**TOTAL : 45 PERIODS**

**REFERENCES:**


1. Thomas Bräunl, Embedded Robotics ,Springer,2018.
2. Grimm, Christoph, Neumann, Peter, Mahlknech and Stefan, Embedded Systems for Smart Appliances and Energy Management , Springer2013.
3. Raj Kamal, *Embedded Systems* - Architecture,. Programming and Design",McGraw-Hill,2010
4. Nilanjan Dey, Amartya Mukherjee, Embedded Systems and Robotics with Open Source Tools, CRC press,2016.
5. Karim Yaghmour, Embedded Android , O'Reilly,2013.
6. Steven Goodwin ,Smart Home Automation with Linux and Raspberry Pi, Apress,2013
7. C.K.Toh, " AdHoc mobile wireless networks", Prentice Hall, Inc,2002.


**Mapping of Course Outcomes (COs) with Program Outcomes (POs) Program Specific Outcomes (PSOs)**

| COs | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
| CO1 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO2 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO3 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO4 | 3 | 3 | 2 | | | | | | | | | | | | |
| CO5 | 3 | 3 | 2 | | | | | | | | | | | | |
| | 3 | High | | | | 2 | Medium | | | | | 1 | Low | | |

| Formative assessment | | | |
|---|---|---|---|
| **Bloom's Level** | **Assessment Component** | **Marks** | **Total marks** |
| Remember | Classroom or Online Quiz | 5 | 15 |
| Understand/ Apply | Class Presentation/Power point presentation | 5 | |
| | Attendance | 5 | |

| Summative Assessment | | | | |
|---|---|---|---|---|
| **Bloom's Category** | **Continuous Assessment Tests** | | | **Terminal Examination (60)** |
| | **IAE 1 (7.5)** | **IAE 2 (7.5)** | **IAE 3 (10)** | |
| Remember | | | | |
| Understand | | | | |
| Apply | 30 | 30 | 30 | 60 |
| Analyze | 20 | 20 | 20 | 40 |
| Evaluate | | | | |
| Create | | | | |